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DEEP-TRENCH 1T-SRAM WITH BURIED OUT DIFFUSION WELL MERGED WITH AN ION IMPLANTATION WELL

Abstract

A deep-trench 1T-SRAM memory cell is disclosed. The deep-trench 1T-SRAM memory cell includes a first conductivity type semiconductor substrate with a main surface. A second conductivity type ion implantation well with a well junction depth is located on the main surface. A gate dielectric layer is located on the ion implantation well. A gate is located on the gate dielectric layer. A heavily doped S/D region of the first conductivity type is disposed at one side of the gate in the ion implantation well. A lightly doped drain (LDD) region of the first conductivity type is disposed at the other side of the gate in the ion implantation well. A deep trench capacitor vertically extends into the main surface through the well junction depth of the ion implantation well to a pre-selected depth. The deep trench capacitor, which is fabricated adjacent to the LDD region, comprises an ion out diffusion well of the second conductivity type that is formed at a lower portion of the deep trench capacitor and is merged with the ion implantation

well. A polysilicon electrode pillar is electrically isolated from the LDD region, the ion implantation well, and the ion out diffusion well by a capacitor dielectric layer and a trench top insulation layer.